QUASI-STATIC FAILURE MODES OF SILICON DIES

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Abstract

In order to guarantee the reliability of semiconductor devices, an optimized package design is required. Depending on the preparation and processing of silicon dies, different flaw populations may be induced, essentially leading to different failure modes during their use. Consequently, such products are characterized by a broad distribution of strengths. Moreover, when subjected to a supercritical loading, brittle silicon develops complex fragmentation patterns, in general preceded by significant deflections. This paper concerns recent progress of numerical simulations of statistically distributed failure and fragmentation. Fracture is described as the progressive separation of two surfaces across the extended crack tip (process zone), resisted by cohesive tractions. In particular we shall use Ball-On-Edge tests to quantify the drop in the load-deflection curve associated with the onset of fracture. Numerical results of plate deflection and failure processes are compared to corresponding experimental results.

1. The problem. The mechanical response of thin structures is a key problem in solid mechanics. Applications range from aeronautics (e.g., airplane constructions) down to micro-electro-mechanical devices (e.g., MEMS, silicon chips and platines). In practical applications of current interest, the behaviour of thin structures ranges from small to large deformations, leading to the onset of damaging processes, localized fracture and global structural failure.

A typical example of brittle fracture, in a thin "plate-like" structure, is the failure of a silicon die (a chip of single crystal silicon) through a Ball-on-Edge test. An experimental program on silicon dies has been performed at the Institute of Mechanics at TU Berlin, with the aim to estimate life expectation of silicon dies [1, 5]. Different fragmentation patterns have been observed. The mechanisms of the different failure modes were not clarified completely by the experiments. Therefore, here we make recourse to numerical simulations to analyze elastically the stress state within a die, and to investigate brittle failure processes accounting for explicit cohesive crack propagation.

2. Probability of failure. A key point of microelectronic component design is the prediction, starting from simple specimen strength data, of the failure probability of a mechanically loaded component. Typically, these experiments are performed using simple geometries, i.e. 3-point-bending tests, where the applied load is increased progressively until fracture occurs. Thus, statistical strength parameters are determined from the collected experimental data. Unfortunately, the traditionally used 3 point-bending tests always lead to a combination of different failure modes and therefore are less applicable for the prediction of maximum tensile stresses. To overcome this issue, a modified bending experiment, the so-called Ball-On-Edge (BoE) test, is adopted here. For brittle materials, such as silicon, the fracture stress can be fitted reasonably well using a two-parameter Weibull distribution

$$P(\sigma) \; = 1 - \exp\left((-\frac{\sigma}{\sigma_L})^m \right) \tag{1}$$

where the reference value σ_L in equation (1) is known as a “scale parameter”, roughly equal to the strength at 63rd percentile of fracture probability, and m is the Weibull coefficient. A high variability of the fracture stress within a particular batch of specimen is characterized by a small Weibull coefficient.

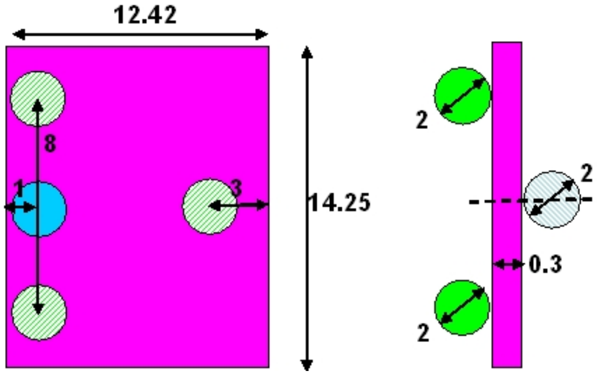


Figure 1: Experimental setup of the BoE tests, dimensions in [mm].

The experimental setup of the Ball-on-Edge test is shown in Figure 1. The dies are supported by 3 spherical supports. The load is applied through a fourth sphere (marked in blue).

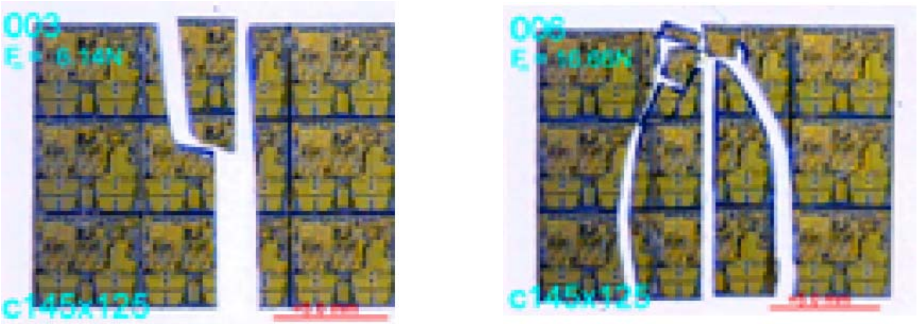


Figure 2: Typical failure pattern of the chip.

A sample program of 20 specimens was subjected to the test. All specimens were loaded until fracture occurred and the loads at fracture were recorded. The fragments of the dies were preserved; two typical fracture patterns are shown in Figure 2.

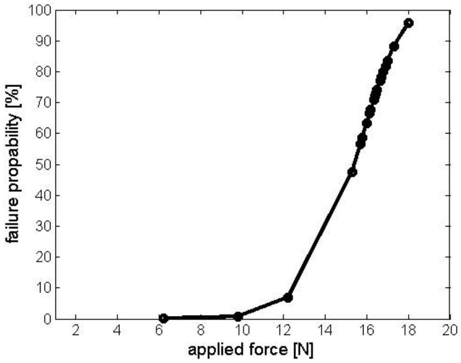


Figure 3: Experimentally determined probability of failure vs. the failure load.

Figure 3 shows the observed distribution of strength data. Obviously, some specimens in the batch fail at very low loads while others are capable of withstanding very high loads. In general, most of the specimens show an intermediate strength. A high quality material should not present high variability in strength. Good products are characterized by a narrow strength distribution, whereas a broad distribution denotes a less advanced material, or even may indicate a processing fault. The graph in Figure 3 does deviate from the typical S-shape of a Weibull distribution in the sense that several specimen fail at very low loads. Clearly, this indicates the existence of a flawed (or otherwise weakened) population of silicon dies. For a better understanding of the mechanisms of low strength failure we proceed to simulate the full BoE test procedure using the finite element method.

3. Numerical simulations. In the elastic finite element analysis we modelled the BoE test setup in a fully three-dimensional manner, see Figure 4. The specimen size is 14.5 x 12.5 x 0.29 mm. It has been meshed with 38500 tetrahedral elements, showing a progressive refinement towards the highly stressed regions. The support and loading spheres are assumed to be rigid. The analysis accounts for large deformations. The material is assumed to deform elastically, i.e., between true stresses σ_{ij} and strains ε_{ij} holds the linear relation:

$$\sigma_{ij} = C_{ijkl}\varepsilon_{kl} \tag{2}$$

Single crystal silicon shows an orthotropic material behaviour and, thus, the fourth order elasticity tensor C_{ijkl} has of only 9 independent entries. Exploiting the cubic symmetry of the crystal lattice yields only 3 different coefficients with values [2]: 165800, 63900 and 79600 MPa. The numerical contour levels of the effective stress (Mises stress) are shown in Figure 4. We clearly see the highly stressed region beneath and at the location of the load driven sphere. Pre-existent defects and heterogeneities at the micro-scale may result in the nucleation of micro-cracks, which in turn coalesce into large structural cracks. Such cracks follow meandering paths and may undergo frequent branching, depending upon the loading and boundary conditions.

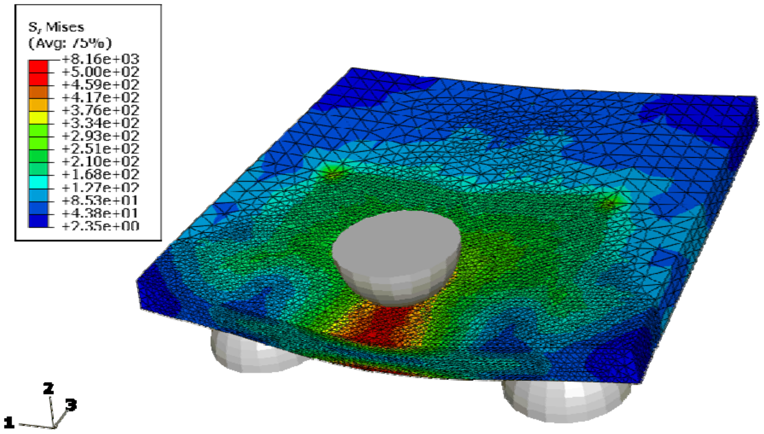


Figure 4: Finite-element mesh and effective von Mises stress in the BoE model.

In order to simulate the actual onset and propagation of cracks we adopt a fragmentation technique based on cohesive element insertion, see [3, 4]. Across the cohesive surfaces, the displacement jump $\boldsymbol{\delta}$ is resisted by cohesive tractions $\mathbf{t}$. Cohesive tractions are linked to the displacement jump through the cohesive law. We postulate the existence of a cohesive free energy density ψ, function of the displacement jump, which acts as a potential for the cohesive tractions:

$$\mathbf{t} = \frac{\partial \Psi(\boldsymbol{\delta}, q)}{\partial \boldsymbol{\delta}} \tag{3}$$

The internal variable q in (3) is included in order to describe the irreversible behaviour of fracture. The cohesive law is modified here in order to account explicitly for the different behaviour in opening and sliding, which appears in mixed mode fracture conditions.

The discretized plate is originally fully coherent, and cohesive surfaces are inserted selectively between solid elements only when a suitable measure of the effective stress, evaluated on the separation surfaces, reaches the resistance threshold. Fractures are described explicitly and, due to the presence of the intrinsic cohesive length scale, spurious mesh dependency effects are avoided.

The numerical simulation displayed in Figure 5 shows the propagation of a central crack in the middle of the chip. The crack enucleates at the position of the point load and propagates towards the front side of the plate and, concurrently, towards the back of the plate until it finally fragments the chip. The colored contour levels in Figure 5 denote the fractured regions, basically indicating rough and damaged free surfaces along the crack path. Note that the displacements shown in the pictures are not scaled.

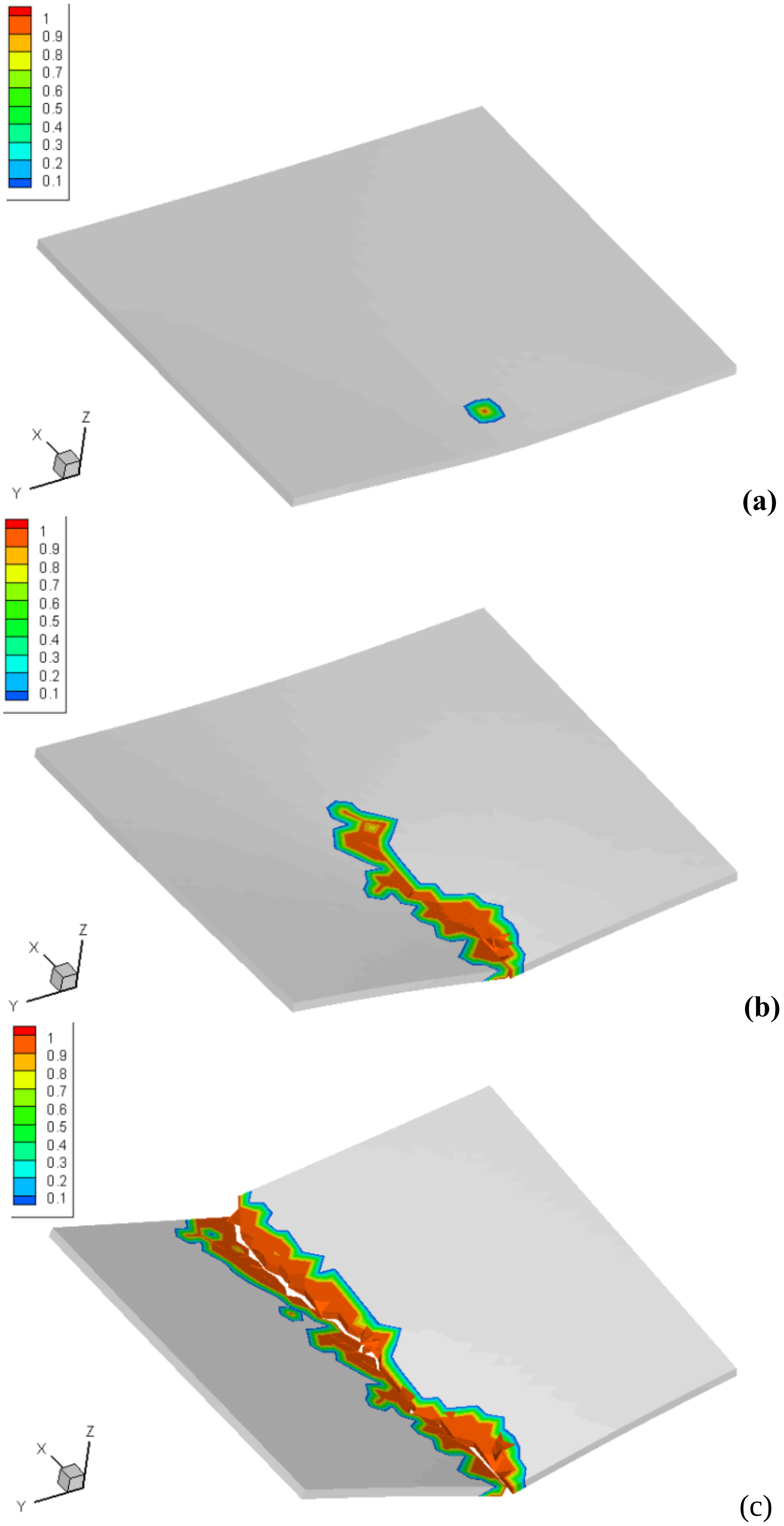
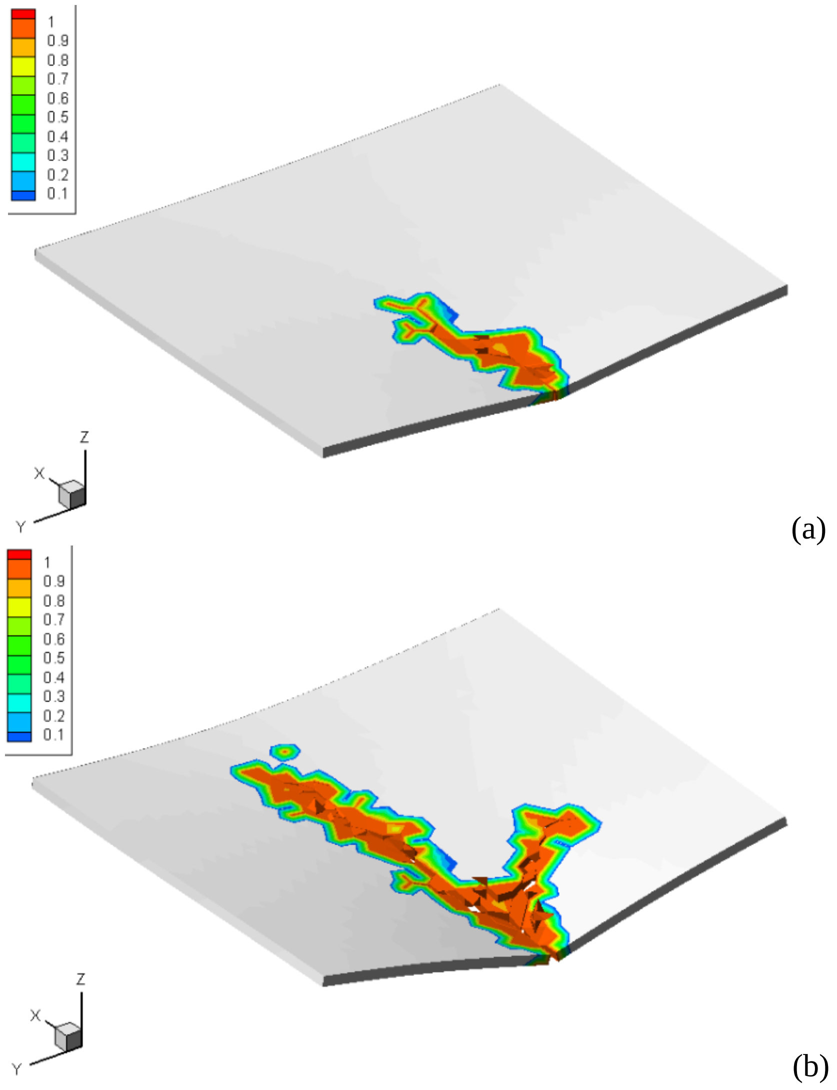


Figure 5: Fracture pattern evolution as obtained in a finite element model of the BoE test assuming the nominal strength for the material. (a) Fracture onset; (b) intermediate situation; (c) final configuration.

The finite element analysis of crack propagation accounts for the full non-linearity of the problem. Tipically, before the onset of fragmentation, a silicon wafer presents a deflection larger than its thickness.



(a)

(b)

Figure 6: Fracture pattern evolution as obtained in a finite element model of the BoE test assuming a flowed material. (a) intermediate configuration; (b) final configuration.

The failure patterns observed in the experiments appear more fragmented than the ones suggested by the numerical simulation. One reason for this discrepancy may be that the notching effects of distributed scratches and microcracks play a major role in the failure of silicon dies. In practice, the dies are already weakened by damaging flaws induced during processing. In order to produce realistic crack pattern in our numerical simulations, we reduced by 30% the stiffness of the die and performed the same static analysis. The new results are shown in Figure 6. The crack branches and propagates simultaneously in two different directions.

Such behaviour indicates a failure starting from the surface of the die, cf. [1] and corresponds to the experimental observation of a failure load below the theoretical limit. Therefore, a weakened (or overall awed) silicon chip may result in branched cracks and more fragmentation.

4. Outlook. The topic of fracture and fragmentation in silicon die is work in progress and further investigations and numerical simulations are ongoing. Nonetheless, we may already state that the highly fragmented patterns correspond to a reduced stiffness of the die and, as observed experimentally, to a reduced maximum load. In future simulations we will study the influence of locally pre-damaged regions (e.g., flaws along the edges) on the failure of the orthotropic silicon wafer. There we expect a further reduction of the failure load.

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