X International Conference on Computational Plasticity
COMPLAS X
E. Oñate and D. R. J. Owen (Eds)

FAILURE MODES OF SILICON DIES

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Key words: Computational Cohesive Fracture, Silicon dies, Fragmentation.

Summary. The reliability of semiconductor devices demands an optimized design of the package. The production process and packaging procedures of silicon dies may induce different flaw populations. Flaw variability causes a broad distribution of strengths and, during the use of silicon devices, leads to different failure modes. Moreover, when subjected to supercritical loadings, brittle silicon develops tortuous fragmentation patterns, in general preceded by significant deflections. As a preliminary investigation in view of a future statistical study, this paper presents recent numerical simulations of quasistatic fracture and fragmentation in silicon dies. Fracture is described as the progressive separation of two surfaces across the extended crack tip (process zone), resisted by cohesive tractions. In particular we refer to Ball-On-Edge tests to quantify the drop in the load-deflection curve associated with the onset of fracture. Numerical results in terms of plate deflection and fracture patterns are compared to the corresponding experimental results.

1 INTRODUCTION

The prediction of the failure probability of a component, starting from the statistical distribution of the strength of simple specimens, is a key point of microelectronic component design. A set of fracture experiments on silicon dies was carried out at the Institute of Mechanics, Technical University of Berlin a few years ago, with the aim to estimate the life expectation of silicon dies. A modified bending experiment, the so-called Ball-On-Edge (BoE) test, has been used to avoid the combination of different failure modes generally observed in the 3-point-bent fracture test. Regrettably, the experiments were not able to clarify the failure mechanisms. They showed a variety of fragmentation patterns, and the corresponding strength distribution deviated from the typical S-shape of a Weibull distribution in the sense that several specimen failed at very low loads, denoting a flawed (or otherwise weakened) population of silicon dies. For a better understanding of the mechanisms of low strength failure, we proceeded to simulate the full BoE test procedure using the finite element method. We carried out two sets of numerical analysis in finite deformations, one elastic, one inelastic accounting for fracture.

2 NUMERICAL ANALYSIS

We initially analyzed the elastic behaviour of one chip, considered as anisotropic plate (according to the material characteristics). The finite element model for this analysis was suitably refined in proximity of the loading points, to capture with precision the stress gradient. The analysis provided the distribution of the stresses in the plate, which were useful to identify the regions of higher stress and the effects of the anisotropy, see Fig. 1 (displacements not amplified).

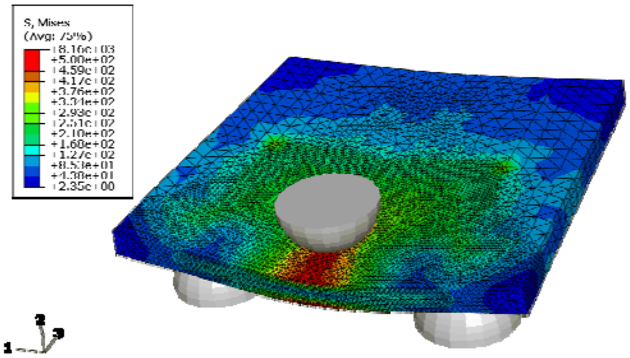

Figure 1: Finite-element mesh and effective von Mises stress in the elastic analysis of the BoE model.

Clearly, in the high stress regions pre-existent defects and heterogeneities present at the micro-scale may result in the nucleation of micro-cracks, in turn with the potential to coalesce into large structural cracks. Such cracks follow meandering paths and may undergo frequent branching, depending on the loading and boundary conditions. In order to simulate the actual onset and propagation of cracks we use a fragmentation adaptive procedure based on the insertion of cohesive elements. The cohesive fracture theory is well understood and generally accepted for analyzing failure of brittle (and in some cases also ductile) materials, undergoing Mode I or mixed Mode failure.

For the fracture analysis, we adopted a different mesh, coarser than the one used for the elastic analysis. The discretized plate is originally fully coherent. Cohesive surfaces, that represent the evolving cracks, are inserted selectively between solid elements when a suitable measure of the effective stress reaches the resistance threshold. Fractures are described explicitly and, due to the intrinsic cohesive length scale, suitably resolved by the discretization, spurious mesh dependency effects are avoided.

The results of the numerical simulation in Fig. 2 show the propagation of a central crack in the middle of the chip. The finite element analysis of crack propagation accounts for the full non-linearity of the problem, and are in agreement with the experimental observations, where a silicon wafer shows a deflection larger than its thickness.

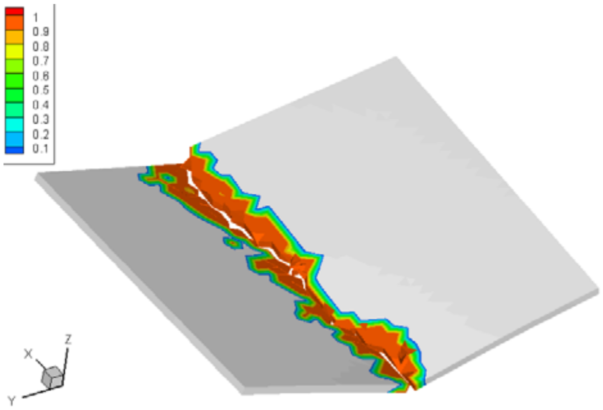

Figure 2: Fracture pattern evolution as obtained in a fracture finite element simulation of the BoE test, assuming the nominal strength for the material.

The actual failure patterns observed in the experiments show more fragments than the ones suggested by the numerical simulation. One reason for this discrepancy may be that notching effects of distributed scratches and microcracks play a major role in the failure of silicon dies. In practice, the dies are already weakened by damaging flaws induced during the processing phase.

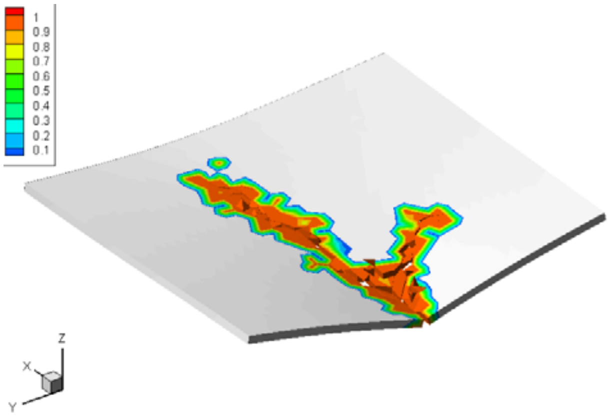

Figure 3: Fracture pattern evolution as obtained in a finite element model of the BoE test assuming a flowed material.

In order to produce more realistic crack patterns, we performed a third numerical simulation of fracture propagation where we reduced by 30% the stiffness of the die, see Fig. 3. The crack branches and propagates simultaneously in two different directions. Such behaviour indicates a failure that starts from the surface of the die and corresponds to the experimental observation of a failure load below the theoretical limit. Therefore, it is likely that a weakened silicon chip will produce more branched cracks and more fragments.

3 CONCLUSIONS

The topic of fracture and fragmentation in silicon die is work in progress. Further investigations and numerical simulations are ongoing. Nonetheless, we may already state that the highly fragmented patterns correspond to a reduced stiffness of the die and, as observed experimentally, to a reduced maximum load. In future simulations we will study the influence of locally pre-damaged regions (e.g., flaws along the edges) on the failure of the orthotropic silicon wafer. There we expect a further reduction of the failure load.

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